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SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
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NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/673,507	STRANG, ERIC J.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-81 has/have been presented for examination based on amendment filed on 19th July 2007.
2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 19th July 2007 has been entered.
3. Claim(s) 78 is/are amended.
4. Claim(s) 1 at least remain rejected under 35 USC § 112.
5. Claim(s) 1 at least remain rejected under Double Patenting with US Patent Applications 10/673,583, 10/673,501 and 10/673,138.
6. Claim(s) 1-21, 29-30, 32-34, 37, 38-58, 66-67, 69-71, and 74-81 remain rejected under 35 USC § 103 with Sonderman in view of Jain.
7. Claim(s) 22 and 59 remain rejected under 35 USC § 103 with Sonderman in view of Jain, further in view of Yunemura.
8. Claim(s) 23-28 and 60-65 remain rejected under 35 USC § 103 with Sonderman in view of Jain, further in view of Chen.
9. Claim(s) 31, 36, 68 and 73 remain rejected under 35 USC § 103 with Sonderman in view of Jain, further in view of Nikoonahad.

10. Claim(s) 35 and 72 remain rejected under 35 USC § 103 with Sonderman in view of Fatke.

11. The arguments submitted by the applicant have been fully considered. Claims 1-81 remain rejected and this action is made NON-FINAL. The examiner's response is as follows.

Response to Applicant's Remarks & Examiner's Withdrawals

12. Examiner withdraws the claim rejection(s) under 35 USC § 101 to claim(s) 78 in view of the amendment and/or applicant's arguments.

Response to Applicant's Remarks for 35 U.S.C. § 103

13. **Claims 1-51 were rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Jain.**

(Argument 1) Applicant has cited Sonderman Col.9 Lines 46-51

> The system 100 then optimizes the simulation (described above) ***to find more optimal process target*** (T.sub.i) **for each silicon wafer, S.sub.i.** ***to be processed.*** These target values are then used ***to generate new control inputs***, X.sub.Ti, on the line 805 to control ***a subsequent process*** **of a silicon wafer S.sub.i [Emphasis added by examiner]**. The ***new control inputs***, X.sub.Ti, are generally based upon a plurality of factors, such as simulation data, output requirements, product performance requirements, process recipe settings based on a plurality of processing tool 120 operating scenarios, and the like.

with the following argument:

> Thus, this section of Sonderman et al clearly discloses that the simulation is to find a more optimum process target for each silicon wafer to be processed. The simulation results produce a new control input for the silicon wafer to be processed. Thus, Applicant respectfully submits that Sonderman et al. teach performing first principles simulation for the actual process to be performed before performance of the actual process, and not the claimed performing first principles simulation ***for the actual process being performed during performance of the actual process.***

(Response 1) Applicant emphasized section of Sonderman is bolded and italicized. Examiner cited portion is bolded and underlined.

Examiner disagrees with the applicant that argument because the results of the simulation are applied to the same semiconductor. Sonderman clearly states each silicon wafer S.sub.i is exposed to new control inputs for subsequent processing (not subsequent wafer in the next round as indicated by second underlined phrase). If the intent of Sonderman not was to indicate that new control inputs generated by simulation for the actual process being performed during performance of the actual process, he would have stated it is applied to the subsequent **silicon wafer S.sub.*i+1.***

Instead the inputs are applied to the same silicon wafer **S.sub.i**. Applicant's arguments are unpersuasive.

(Argument 2) Applicant has cited Fig.4 from Sonderman requiting the steps in Fig.4 and presenting the following argument.

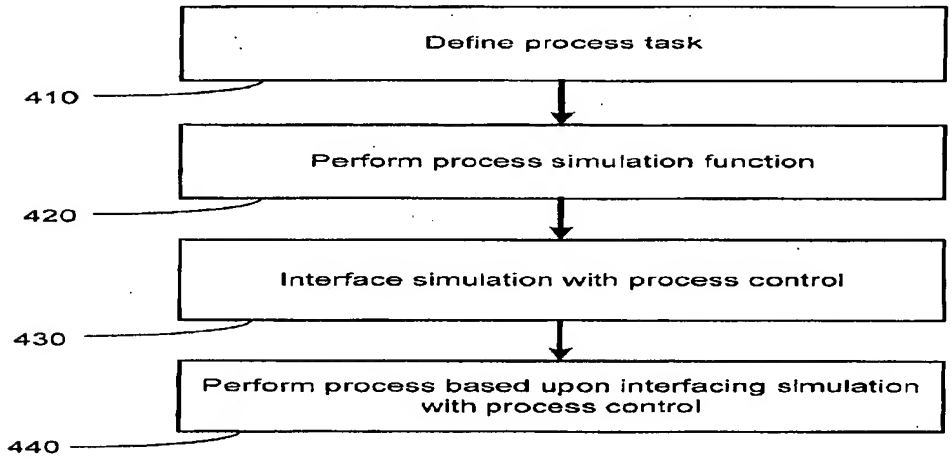

FIGURE 4

Hence, the process flow in Sonderman et al is straightforward:
1) define process to be modeled,
2) model process for simulation result,
3) interface simulation result to processor, and then
4) run the process under control based on the pre-existing simulation result.

Note also that this sequence in Sonderman et al means that Sonderman et al do not disclose inputting process data relating to an actual process being performed by the semiconductor

processing tool, as also claimed. Rather, Sonderman et al use data from previous runs to produce a simulation result.

Accordingly, Applicant respectfully submits that Sonderman et al do not disclose and indeed teach away from the present invention.

(Response 2) Examiner thanks applicant for their interpretation, however the interpretation is incomplete with the reference that this process involves a feedback, therefore the applicant's assertion that control is based on the pre-existing simulation result and Sonderman et al does not disclose inputting process data relating to an actual process being performed by the semiconductor processing tool is incorrect. Sonderman Col.4 Line 65-Col.5 Line 10 states:

> Furthermore, the simulation environment 210 can be used for feedback modification of control parameters invoked by the process control environment 180. For example, the manufacturing environment 170 can send metrology data results into the simulation environment 210. The simulation environment 210 can then use the metrology data results and perform various tests and calculations to provide more accurate, modified control parameters to the process control environment 180. A feedback loop in then completed when the process control environment 180 sends the modified or adjusted process control parameters to the manufacturing environment 170 for further processing of semiconductor wafers.

Sonderman clearly teaches inputting process data relating to an actual process being performed by the semiconductor processing tool, into the simulator and applying the simulation result to the semiconductor-processing tool.

Further in support of examiner's argument, applicant is also performing the same process of feedback modification (See specification Fig.7). In conclusion, Sonderman does not teach away from the claimed invention and applicant's arguments are found to be unpersuasive.

(Argument 3) Applicant has argued that Jain does not overcome the deficiencies of Sonderman.

(Response 3) Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Applicant has merely cited portion of Jain without clearly showing why Jain does not overcome the deficiencies of Sonderman.

(Argument 4) Applicant has stated the following:

> Moreover, the proposed development work in Jain is understood better in the light of the "conventional approach" referred to by Kee et al, made of record by the Information Disclosure Statement filed December 20, 2005.

Further arguments are presented with current case law KSR International Vs. Teleflex Inc.

(Response 4) First, Kee et al is not used as prior art for rejecting the current invention. Secondly, examiner fails to see the connection between Jain and Kee et al as neither of them reference to each other in any way. Thirdly, Applicant also has not further established why the so-called "conventional approach" would link them. In light of the above applicant's arguments are found to be unpersuasive.

(Argument 5) Applicant has argued:

> In the present situation, the claimed method of performing a first principles simulation for the actual process being performed during performance of the actual process produces more than an expected result in that Sonderman et al (***in having to develop a new control inputs for each subsequent wafer***) can not compensate for real time excursions from the existing model occurring while the wafer is being processed. In other words, the lengthy time for generation of a first principles model simulation in the prior art prevents one from realizing a real time process control based on a first principles simulation during the actual process. Indeed, as pointed out above, the examiner considered it an impossibility to simultaneously perform a first principles simulation result and to control the actual process being run with the first principles simulation result. Hence, the claimed processes and systems produce an unexpected result.

(Response 5) Examiner thanks applicant for the remarks above, however the new control inputs are not developed for the processing of each subsequent wafer, but

instead are for subsequent processing [performed on] a silicon wafer S.sub.i (Sonderman: Col.9 Lines 44-46 – this point is also addressed above in response to argument 1).

Further ***most importantly*** applicant is arguing limitation, which are not present in the claim and may constitute patentable subject matter. Specifically, as indicated by applicant "the lengthy time for generation of a first principles model simulation in the prior art prevents one from realizing a real time process control based on a first principles simulation during the actual process." However, this is the conclusory statement, where what makes the current first principle simulation model realize the real time process control possible is not claimed. Further distinguishing it from Sonderman may also help in defining a more patentable subject matter.

Claim Rejections - 35 USC § 112¶1st and response the applicant's remarks

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

14. Claim 1-81 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Exact details of what basic physical and chemical attribute of the semiconductor processing tool are used to construct a first principle simulation model which is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Applicant has argued citing specification paragraphs [0035] and [0036] as to what constitutes first principle physical model.

(Response to applicant's remarks)

Applicant has provided an exact support in disclosure for such attributes in the model. Applicant has incorrectly quoted specification paragraphs [0035] and [0036]. These paragraph are not enabling although they rely on the commercially available packages to model the various first principle simulation models, the details of the model are absent from the specification. The details of these model which lead to unexpected results (Argument & response 5) are very relevant to the designing the first principle physical model. Examiner respectfully maintains the rejection.

Response to Applicant's Remarks for Double Patenting

15. Applicant's arguments relating to filing a terminal disclaimer for applications 10/673,501, 10/673,507 and 10/673,583 are considered and double patenting rejection is maintained until a terminal disclaimer is filed.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

16. Claim 1 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,507 (Updated 9/19/06).

Application No. 10/673,501	Application No. 10/673,507
A method of facilitating a process performed by a semiconductor processing tool, comprising:	A method of controlling a process performed by a semiconductor processing tool, comprising:
inputting data relating to a process performed by the semiconductor processing tool;	inputting data relating to a process performed by the semiconductor processing tool;
inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;	inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attributes of the semiconductor processing tool;
performing first principles simulation for the actual process being performed *during performance of*	performing first principles simulation for the actual process being performed *during performance of*

actual process using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed; and	*actual process* using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed; and
using the simulation result *obtained during performance of actual process* as part of a data set that characterizes the actual process being performed by the semiconductor processing tool.	using the first principles simulation result *obtained during performance of actual process* to control the actual process performed by the semiconductor processing tool.

Although the conflicting claims are not identical, they are not patentably distinct from each other because both the virtual sensor measurements are the same simulation result (Specification: Page 13[0051] Last sentence). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

17. **Claim 1 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,583 (Updated 9/19/06).**

Application No. 10/673,501	Application No. 10/673,583
A method of facilitating a process performed by a semiconductor processing tool, comprising:	A method of facilitating a process performed by a semiconductor processing tool, comprising:
inputting data relating to a process performed by the semiconductor processing tool;	inputting data relating to a process performed by the semiconductor processing tool;
inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;	inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;
performing first principles simulation for the actual process being performed *during performance of actual process* using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed; and	performing first principles simulation for the actual process being performed *during performance of actual process* using the physical model to provide a virtual sensor measurement in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed; and
using the simulation result *obtained during performance of actual process* as part of a data set that characterizes the actual process being performed by the semiconductor processing tool.	using the virtual sensor measurement *obtained during performance of actual process* to facilitate the actual process performed by the semiconductor processing tool.

Although the conflicting claims are not identical, they are not patentably distinct from each other because both claims perform the same steps and use the simulation result to control the semiconductor-processing tool. Characterization is similar to controlling (Specification: Page 6[0032]). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

18. **Claim 1 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,138 (Updated 9/19/06).**

Application No. 10/673,501	Application No. 10/673,138
A method of facilitating a process performed by a semiconductor processing tool, comprising:	A method of facilitating a process performed by a semiconductor-processing tool, comprising:
inputting data relating to a process performed by the semiconductor processing tool;	inputting data relating to a process performed by the semiconductor processing tool;
inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;	inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;
performing first principles simulation for the actual process being performed *during performance of actual process* using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed; and	performing first principles simulation for the actual process being performed *during performance of actual process* using the physical model to provide a first principles simulation result in accordance With the process data relating to the actual process being performed in order to simulate the actual process being performed; and
using the simulation result *obtained during performance of actual process* as part of a data set that characterizes the actual process being performed by the semiconductor processing tool.	using the first principles simulation result *obtained during performance of actual process* to facilitate the actual process being performed by the semiconductor processing tool.

Although the conflicting claims are not identical, they are not patentably distinct from each other because both claims perform the same steps and use the simulation result to control/facilitate the semiconductor-processing tool. Facilitating is also similar to controlling (Specification: Page 6[0032]). This is a provisional obviousness-

type double patenting rejection because the conflicting claims have not in fact been patented.

Further, all the three non-statutory obviousness-type double patenting rejections for the application have substantially same or identical specification. Also, independent claims belonging different statutory category, having substantially similar limitations, in the three co-pending applications may also have similar double patenting rejections.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

19. Claims 1-21, 29-30, 32-34, 37, 38-58, 66-67, 69-71, and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter).

Regarding Claim 1

Sonderman teaches a method to controlling a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17;Col.3 Lines 45-49) by inputting *process* data relating to *an actual* process *being* performed by the semiconductor-processing tool (Sonderman: at least in Col.3 Lines 50-67; *Col.7 Lines 8-20*). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool *describing at least one of a basic physical or chemical attributes* (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation *for the actual process being performed* during performance of actual process *(Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63,* Fig.1-3*)* using the physical model to *provide simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed* (Sonderman: at least in Col.5-7). Further, Sonderman teaches using the first principle simulation results *obtained during the performance of the actual process* (Sonderman: Fig. 1-3 *Col.7 Lines 4-7; Col.3 Lines 56-63)* to control the process performed by the semiconductor-

processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8; Col.2 Lines 10-17).

Sonderman does not teach first principle model including a set of computer encoded differential equations.

Jain teaches computer encoded differential equations using MPE engine, which can be applied to wafer processing (Jain: Abstract). Jain also teaches dedicated and wafer level implementation of MPE engine to provide enhanced performance (Jain: Pg. 372 Section V Dedicated MPE).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Jain to Sonderman to solve differential equation for the semiconductor processing tool. Sonderman teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (Sonderman: Fig.1; Col.7 Lines 8-20), while Jain makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (Jain: Abstract).

Regarding Claim 2

Sonderman teaches directly inputting the *process* data relating to the *actual* process *being* performed by the semiconductor-processing tool from at least one of physical sensor (e.g. Scatterometry data, overlay data, dimensional data) and a metrology tool physically mounted on the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; *Col.7 Lines 8-20*).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the *process* data relating to the *actual* process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator (Sonderman: at least in Fig.1-3 Col.1; Col.4-7; Col.7 Lines 8-20).

Regarding Claims 6-9

Sonderman teaches inputting process data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at east on of the characteristics and a result of a process performed by the semiconductor processing tool; inputting a spatially resolved model (as modified models) of the geometry of the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation result (Sonderman: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3; Col.7 Lines 8-20). Sonderman and Jain teach inputting fundamental equations as the set of computer encoded differential equations (Sonderman: Col.9 (equations); Jain: Pg. 372 Section V Dedicated MPE, Abstract).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63).

Regarding Claims 11-13

Sonderman teaches performing first principle simulation independent of the process performed by the semiconductor-processing tool; inputting data from to set initial & boundary condition on the first simulation model (Sonderman: at least in Col.5-8; Fig.3-4).

Regarding Claim 14

Sonderman teaches using the first principles simulation result comprises using the first principles simulation result to perform at least one of detecting, and classifying a fault in the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5 Line 56 – Col.6 Line 24).

Regarding Claims 15-19

Sonderman teaches using a network of interconnected resources *inside the semiconductor manufacturing facility (Sonderman: Semiconductor tools on the factory floor – Col.9 Lines 60-65)* to perform *first principle simulation (Jain: Section III)*; using code parallelization among interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool; sharing simulation results among the interconnected

resources to reduce redundant execution of substantially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 20-21

Sonderman teaches remote access to computational and storage resources (Sonderman: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 29

Sonderman teaches performing a principle components analysis to determine a relationship between spatial components of said first principles simulation result for the semiconductor processing tool and a set of at least one control variable, said relationship utilized to determine a correction to said set of at least one control variable in order to affect a reduction in the magnitude of said spatial components (Sonderman: Col.5 Line 56 – Col.6 Line 23).

Regarding Claim 30

Sonderman teaches first principle simulation controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: at least in Col 4 Lines 18-31; Col.3 Lines 45-49).

Regarding Claim 32

Sonderman teaches inputting various parameters *as tool data* relating to etching, deposition etc. (Sonderman: at least in Col.5 Lines 56-67).

Regarding Claim 33

Sonderman teaches inputting physical geometric data as parameters for the equipment model where the equipment could be at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: Col.5 Lines 56-67).

Regarding Claim 34

Sonderman teaches first principles simulation result controlling the semiconductor processing tool by using model output to adjust said process performed by the semiconductor processing tool (Sonderman: Col.4 Lines 48-64; Fig.1-2).

Regarding Claim 37

Sonderman teaches inspecting process results and providing input to the first principles simulation for calibration purposes (Sonderman: Col.6 Lines 14-24).

Regarding Claim 38

System claim 38 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 39

System claim 39 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claims 40-42

System claims 40-42 disclose similar limitations as claims 3-5 and are rejected for the same reasons as claims 3-5 respectively.

Regarding Claims 43-46

System claims 43-46 disclose similar limitations as claims 6-9 and are rejected for the same reasons as claims 6-9 respectively.

Regarding Claim 47

System claim 47 discloses similar limitations as claim 10 and is rejected for the same reasons as claim 10.

Regarding Claims 48-50

System claims 48-50 disclose similar limitations as claims 11-13 and are rejected for the same reasons as claims 11-13 respectively.

Regarding Claim 51

System claim 51 discloses similar limitations as claim 14 and is rejected for the same reasons as claim 14.

Regarding Claims 52-56

System claims 52-56 disclose similar limitations as claims 15-19 and are rejected for the same reasons as claims 15-19 respectively.

Regarding Claims 57-58

System claims 57-58 disclose similar limitations as claims 20–21 and are rejected for the same reasons as claims 20-21 respectively. *Change in dependency from claim 52 to claim 38 of claim 57 is noted.*

Regarding Claim 66

System claim 66 discloses similar limitations as claim 29 and is rejected for the same reasons as claim 29.

Regarding Claim 67

System claim 67 discloses similar limitations as claim 30 and is rejected for the same reasons as claim 30.

Regarding Claim 69

System claim 69 discloses similar limitations as claim 32 and is rejected for the same reasons as claim 32.

Regarding Claim 70

System claim 70 discloses similar limitations as claim 33 and is rejected for the same reasons as claim 33.

Regarding Claim 71

System claim 71 discloses similar limitations as claim 34 and is rejected for the same reasons as claim 34.

Regarding Claim 74

System claim 74 discloses similar limitations as claim 37 and is rejected for the same reasons as claim 37.

Regarding Claim 75 (Updated)

System claim 75 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 76 (Updated)

System claim 76 discloses similar limitations as claim 16 and is rejected for the same reasons as claim 16. Sonderman teaches sharing *inside the semiconductor device manufacturing facility (Sonderman: Semiconductor tools on the factory floor – Col.9 Lines 60-65*) the computational load (also see APC).

Regarding Claim 77

System claim 77 discloses similar limitations as claim 17 and is rejected for the same reasons as claim 17.

Regarding Claim 78 (Updated)

Article of manufacture claim 78 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claims 79-81

Jain teaches use of Navier Stokes and other known simulation solutions for solving various simulation problems as initial condition (Jain: Pg. 367-368 Section "Governing Rationale" Sub-Section A. Governing Equations). Sonderman also teaches initializing the models with input data (Sonderman: Col.7 Lines 8-20).

20. Claims 22 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), further in view of IEEE article "Heat Analysis on Insulated Metal Substrates" by Naomi Yunemura et al (Yunemura hereafter).

Regarding Claim 22

Teachings of Sonderman and Jain are disclosed in claim 1 rejection above. Sonderman also teaches that the first principle simulation models the equipment conditions, thereby modeling temperature response and pressure response during various processes (Sonderman: at least in Col.5 Lines 62-67). Jain also teaches distributed and dedicated hardware implementation to solving wafer problem using computer implemented differential equations (Jain: Section III & IV).

Sonderman and Jain do not teach explicitly that such temperature and pressure modeling is done using ANSYS computer code.

Yunemura teaches that heat simulation modeling can be performed using ANSYS computer code (Yunemura: Pg. 1407 Section 1) on a silicon chip.

Motivation to combine Jain with Sonderman is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Yunemura to Sonderman and Jain to create a equipment model as disclosed by Sonderman. The motivation to combine would have been that Yunemura teaches heat modeling on a silicon chip

affecting the thermal conductivity (Yunemura: Pg.1407 Section 2) based on various thicknesses and Sonderman is solving the same issue for the equipment model that for example model the equipment for depositing the various layers and affects on heat and pressure. Further, ANSYS is known in art to be used as thermal & pressure modeling tool based on finite element analysis. Motivation to combine Jain and Yunemura is that Jain as taught above indicates distributed solving of computer implemented differential equations which Yunemura solves by ANSYS modeling, thereby facilitating in implementation of Jain's teachings.

Regarding Claim 59

System claim 59 discloses similar limitations as claim 22 and is rejected for the same reasons as claim 22.

21. Claims 23-28 and 60-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), further in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter).

Regarding Claims 23-25

Teachings of Sonderman and Jain are disclosed in claim 1 rejection above.

Sonderman and Jain does not explicitly teach close fitting the solution of the first principle simulation run to thereby set initial conditions for cells in the first principle simulation; selecting close fitting solutions from a library based on convergence.

Chen teaches close fitting the solution of the first principle simulation run to thereby set initial conditions for cells in the first principle simulation; selecting close fitting solutions from a library based on convergence (Chen: at least in Col.5 Lines 38 – Col.6 Line 25; Fig 3A-B).

Motivation to combine Jain with Sonderman is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Chen to Sonderman and Jain. The motivation to combine would have been that Chen and Sonderman both are analogous art concerned with simulating the semiconductor fabrication process and providing the best control parameters to the actual semiconductor-processing tool (Chen: at least in Col.3 Lines 19-23).

Regarding Claim 26

Chen teaches that the close-fitting solution library existing on a network of computers connected to semiconductor-processing tool (Chen: Fig.2; Col.4 Line 55 –Col.6 Line 19).

Regarding Claims 27-28

Chen teaches calculating solution to the first principle simulation by choosing a coarse grid for solution to the first principle simulation (Chen: at least in Col.6 Line 44-Col.7 Line 14) as user defined parameters; further, subsequent solutions by setting the initial conditions to fine grid are made though Gaussian distribution and actual inline data (Chen: at least in Col.6 Line 46-51).

Regarding Claims 60-62

System claims 60-62 disclose similar limitations as claims 23-35 and are rejected for the same reasons as claims 23-25 respectively.

Regarding Claim 63

System claim 63 discloses similar limitations as claim 26 and is rejected for the same reasons as claim 26.

Regarding Claims 64-65

System claims 64-65 disclose similar limitations as claims 27-28 and are rejected for the same reasons as claims 27-28 respectively.

22. Claims 31, 36, 68 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), in view of U.S. Patent No. 6,812,045 issued to Mehrdad Nikoonahad (Nikoonahad hereafter).

Regarding Claim 31

Teachings of Sonderman and Jain are disclosed in claim 1 rejection above. Sonderman provides examples of the processing tool as etch and photolithography tools (Col.4 Lines 26-31) but does not explicitly disclose chemical vapor and physical vapor deposition system.

Nikoonahad teaches deposition tools to include chemical vapor and physical vapor deposition system (Nikoonahad: Col.24 Lines 3-49).

Motivation to combine Jain with Sonderman is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Nikoonahad to Sonderman and Jain. The motivation to combine would have been that Nikoonahad and Sonderman are analogous art and both are modeling the semiconductor processing and providing feedback to the semiconductor processing tool (Sonderman: Abstract; Nikoonahad: Col.3; Col.93 Lines 20-35).

Regarding Claim 36

Nikoonahad teaches plurality of computing (as processor)/ storage (as memory) devices connected over network to exchange information between a plurality of computing/storage devices including at least one of model solver parameters, solution status to the first principles simulation, model solutions to the first principles simulation, and solution convergence history for said model solutions (Nikoonahad: Col.3 Lines 15-44; Col.68, Lines 41-59).

Regarding Claim 68

System claim 68 discloses similar limitations as claim 31 and is rejected for the same reasons as claim 31.

Regarding Claim 73

System claim 73 discloses similar limitations as claim 36 and is rejected for the same reasons as claim 36.

23. Claims 35 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Application 10/472,436 filed by David Fatke et al. (Fatke hereafter).

Regarding Claim 35

Teachings of Sonderman and Jain are disclosed in claim 1 rejection above.

Sonderman and Jain do not teach step of controlling by utilizing at least on of non-linear optimization and multivariate analysis to derive the control model for the process control.

Fatke teaches utilizing at least on of non-linear optimization and multivariate analysis to derive the control model for the process control (Fatke: [0011][0012][0035][0050]-[0058][0021]). Fatke uses the partial least square (PLS) model to perform multivariate analysis ([0050] to derive the control model for the process control and provide output to the semiconductor-processing tool ([0021]). Further, Fatke teaches that the nonlinear optimization is known in the art for creating such models ([0012]).

Motivation to combine Jain with Sonderman is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Fatke to Sonderman and Jain. The motivation to combine would have been that Fatke and Sonderman are analogous art and Fatke creates a model form the determining the endpoint of the

etching in an etch reactor (Fatke: Abstract/Summary), thereby creating a equipment model and the process model for etching, which can be applied to Sonderman.

Regarding Claim 72

System claim 72 discloses similar limitations as claim 35 and is rejected for the same reasons as claim 35.

Conclusion

1. All claims are rejected.
2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
3. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

   In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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